REMARKS

Double Patenting Rejection

Claims 1-21 were provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-20 of copending U.S. Patent Application Serial No. 09/943,475, in view of *Baltz et al.* (U. S. Patent No. 6,058,474).

The claims of SN 09/943,475 are to a system that has a processor adapted to write compressed data and memory with a decompression circuit that is coupled to receive the compressed data. While Applicant still believes that this is a non-obvious variation of the present claims, a terminal disclaimer has been included with this response in the interest of expediency.

Claim Rejections Under 35 U.S.C. § 102

Claims 1-3, 5, 11, 12, 15, 18 and 21 were rejected under 35 U.S.C. § 102(e) as being anticipated by *Baltz et al.* Applicant respectfully traverses this rejection.

Claims 1, 6, 11, 16, and 19 – 21 have been amended to more clearly claim the subject matter that Applicant regards as the invention. The amended claims make it clear that data is loaded from the non-volatile memory to the volatile memory without intervention by a processor or direct memory access (DMA) circuit.

Baltz et al. discloses using DMA circuitry 100 to transfer data from an 8-bit EPROM 671 to internal program memory 23 as is illustrated in Figure 8. Applicant's invention, as claimed in the amended claims, does not require such intervention. Data from non-volatile memory is transferred directly to volatile memory independent of the processor or DMA circuitry. Therefore, Applicant's invention as claimed is neither taught nor suggested by *Baltz et al.*

Claim Rejections Under 35 U.S.C. § 103

Claims 4, 6-9, 14, and 16-19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Baltz et al.* in view of *Harari et al.* (U.S. Patent No. 6,266,724). Claim 13 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Baltz et al.* in view of *Shin* (U.S. Patent No. 6,735,669). Claims 10 and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Baltz et al.* in view of *Harari et al.* as applied to claims 6 and 19, and further in view of *Shin*. Applicant respectfully traverses this rejection.

Harari et al., in Figure 7, discloses a flash EEPROM connected to a mother card over a serial connection. *Harari et al.* neither teaches nor suggests Applicant's invention as claimed in

the amended claims. Even if it were obvious to combine *Baltz et al.* with *Harari et al.*, and Applicant maintains that it is not, the combination would not teach or suggest Applicant's invention as claimed.

Shin discloses a Rambus RAM that has various modes for low power system operation. *Shin* neither teaches nor suggests Applicant's invention as claimed in the amended claims. Even if it were obvious to combine *Shin* with *Baltz et al.* and or *Harari et al.*, and Applicant maintains that it is not, the combinations would not teach or suggest Applicant's invention as claimed.

CONCLUSION

Applicant respectfully requests that the Examiner enter the present amendment, withdraw the final rejection and allow the claims of the present application. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211. No new matter has been added and no additional fee is required by this amendment and response.

Respectfully submitted,

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